REMARKS

This Amendment responds to the Office Action mailed September 1, 2006 in the above-identified application. Based on the foregoing amendments and the following comments, reconsideration and allowance of the application are respectfully requested.

Claims 1-15 were previously pending the application. By this amendment, claims 1, 3, 7, 12 and 14 have been amended. Claims 2, 4-6, 8, 9 and 13 have been cancelled without prejudice or disclaimer. Accordingly, claims 1, 3, 7, 10-12, 14 and 15 are currently pending, with claims 1, 7 and 12 being independent claims. No new matter has been added.

The Examiner has rejected claims 1, 7, 8, 10, 11, 12 and 15 under 35 U.S.C. §103(a) as unpatentable over Heath et al. (U.S. 4,901,234) in view of Bowes et al. (U.S. 5,655,151). Claims 2, 9 and 13 are rejected under 35 U.S.C. §103(a) as unpatentable over Heath in view Bowes as applied to claims 1, 7 and 12, further in view of Solomon et al. (U.S. 2004/0215868). It appears that the Examiner intended to include claims 2-6, 9, 13 and 14 in the rejection based on Heath in view of Bowes and Solomon. The rejections are respectfully traversed in view of the amended claims.

Heath discloses a computer system including a plurality of peripherals requiring DMA access. Some of the peripherals are allotted fixed, dedicated ones of the DMA channels, while others of the peripherals share the remaining DMA channels. The shared DMA channels are programmable (col. 2, lines 34-46). Heath discloses in Fig. 1 a decentralized arbitration circuit, including a central arbitration control circuit 11 associated with the DMA controller 12 and an arbitration circuit in each of the peripherals (col. 3, lines 33-46).

Bowes discloses a DMA controller having multiple channels, each having multiple register sets storing control information. A single DMA channel of the DMA controller is shown in FIG. 3 of Bowes.

Solomon discloses a storage processor for a disk array system. The storage processor shown in Fig. 2C of Solomon includes a crossbar switch and a DMA/XOR engine in a single ASIC. The crossbar switch links buses 34 and 35 with a memory 39 (paragraph 0035).

Amended claim 1 is directed to a DMA controller comprising, in part, a prioritizer including a priority crossbar configured to map inputs to outputs based on programmable mapping information, wherein the priority crossbar is configured to map DMA requests and DMA grants in response to programmable mapping information associated with each of the DMA channels.

The Examiner assets that Solomon teaches a DMA controller with a crossbar and thereby provides the teachings that are lacking in Heath and Bowes. This assertion is respectfully traversed. Solomon discloses a storage processor wherein a crossbar switch links buses 34 and 35 to a memory 39. The buses carry data (paragraph 0032). Thus, the crossbar disclosed in Solomon *switches data* between buses 34 and 35 and memory 39, and does not establish priority of one data source over another. By contrast, amended claim 1 requires a priority crossbar configured to *map DMA requests and DMA grants in response to programmable mapping information associated with each of the DMA channels.*

Further, the crossbar switch and the DMA/XOR engine 38 shown in Fig. 2C of Solomon are located in a single ASIC. However, Solomon contains no disclosure or suggestion that the crossbar switch is part of the DMA controller or is functionally associated with the DMA controller. The ASIC is simply an integrated circuit that contains the crossbar switch and the DMA/XOR engine. Thus, Solomon provides no basis for asserting that the disclosed crossbar switch would be incorporated into the DMA controller of Heath. The crossbar switch of Solomon does not map DMA requests and DMA grants as claimed. Accordingly, the cited references, taken individually or in combination, do not disclose or suggest a prioritizer configured to map DMA requests from different DMA requesters to DMA channels in response to programmable mapping information, wherein the prioritizer comprises a priority crossbar configured to map inputs to outputs based on the programmable mapping information and wherein the priority crossbar is configured to map

DMA requests and DMA grants in response to programmable mapping information associated with each of the DMA channels, as claimed.

Heath discloses a decentralized arbitration circuit, in contrast to the centralized priority crossbar of amended claim 1. For at least these reasons, amended claim 1 is clearly and patentably distinguished over Heath in view of Bowes and Solomon, and withdrawal of the rejection is respectfully requested. Claim 3 depends from claim 1 and is patentable over the cited references for at least the same reasons.

Amended claim 7 is directed to a method for DMA transfer and requires, in part, mapping DMA requests from different DMA requesters to DMA channels to in response to programmable mapping information and mapping DMA grants from the DMA channels to respective DMA requesters, wherein mapping DMA requests and mapping DMA grants comprises mapping DMA requests and grants with a priority crossbar.

As discussed above in connection with claim 1, the cited references contain no disclosure or suggestion of a DMA controller including a priority crossbar as claimed. For these reasons and for the reasons discussed above in connection with claim 1, amended claim 7 is clearly and patentably distinguished over Heath in view of Bowes and Solomon.

Claims 10 and 11 depend from claim 7 and are patentable over the cited references for at least the same reasons as claims 1 and 7.

Amended claim 12 is directed to a DMA controller and requires, in part, a first prioritizer configured to arbitrate among DMA requests in accordance with a predetermined assignment of priorities, and a second prioritizer configured to map DMA requests from different DMA requesters to DMA channels in response to programmable mapping information, wherein the second prioritizer comprises a priority crossbar configured to map DMA requests to the DMA channels configure to map DMA grants to respective DMA requesters.

As discussed above, the cited references to not disclose or suggest a DMA controller including a prioritizer comprising a priority crossbar as claimed. For these reasons and for the reasons discussed above in connection with claims 1 and 7, amended claim 12 is clearly and patentably distinguished over Heath in view of Bowes and Solomon, and withdrawal of the rejection is respectfully requested.

Claims 14 and 15 depend from claim 12 and are patentable over the cited references for at least the same reasons as claims 1, 7 and 12.

Based upon the above discussion, claims 1, 3, 7, 10-12, 14 and 15 are condition for allowance.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

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Respectfully submitted,

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